Commercial Mobile LPDDR4 8Gb/16Gb(DDP)/32Gb(QDP) SDRAM

Features

- **Basis LPDDR4 Compliant**
  - Low Power Consumption
  - 16n Prefetch Architecture and BL16, BL32 (OTF)
- **Signal Integrity**
  - Internal VREF and VREF Training
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240Ω± 1%)
  - Data bus inversion (DBI)
- **Training for Signals' Synchronization**
  - DQ Calibration offering specific DQ output patterns
- **Data Integrity**
  - DRAM built-in Temperature Sensor for Temperature Compensated Self Refresh (TCSR)
  - Auto Refresh and Self Refresh Modes
- **Power Saving Modes**
  - Partial Array Self Refresh (PASR)
  - Frequency Set Point(WR/OP)
  - Clock-stop capability
- **LVSTL interface and Power Supply**
  - VDD1/VDD2/VDDQ = 1.8V/1.1V/1.1V

Programmable

- **R_{ON} (Typical:40/48/60/80/120/240)**
- **R_{TT} (40/48/60/80/120/240)**
- **RL/WL Select (Set A / Set B)**
- **nWR (X16 mode)**
- **PASR (bank/segment)**

Options

- **Speed Grade (DataRate)**
  -4267 Mbps / RL=36
  -3733 Mbps / RL=32
- **Temperature Range (*Tc*)**
  - Commercial Grade : - 30℃ to +105℃
- **Package Information**
  Lead-free RoHS compliance and Halogen-free

Items (FBGA Package)	Width x Length x Height (mm)	Ball pitch (mm)
200 Ball (SDP/DDP)	10.00 x 15.00 x 1.00	0.65/0.80 Mixed
200 Ball (QDP)	10.00 x 15.00 x 1.20	0.65/0.80 Mixed

- **Density and Addressing**

Items		X16	X16	X16
Die Quantity		Single Die	Dual Die	Quad Die
Number of Banks		8	8	8
Bank Address		BA[2:0]	BA[2:0]	BA[2:0]
Row		R[15:0]	R[15:0]	R[15:0]
Column		C[9:0]	C[9:0]	C[9:0]
tREFI [1]	Tc≦85℃	3.9μs		
	85℃<Tc≦95℃	1.95μs		
	95℃<Tc≦105℃	0.975μs		

如需获取完整版规格书
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